Fully Integrated GPS Receiver Engine Module ORG4475 Data Sheet

1. Introduction

1.1 About the ORG4475

The new OriginGPS GPS module has been designed to target applications where supreme small size and highest level of integration must be coupled with high sensitivity and low power.

The ORG4475 is industry's smallest, autonomous, fully featured GPS module.

Sized only 5.6mm x 5.6mm the record-breaking ORG4475 module is a further miniaturization of the OriginGPS popular ORG447X series.

The ORG4475 module is a multi-channel receiver that continuously tracks all GPS satellites in view and provides accurate positioning data in industry's standard NMEA format.

Featuring OriginGPS Noise-Free Zone System™ technology the ORG4475 module offers the ultimate of satellite navigation in smallest size.

The ORG4475 module is a complete SiP (System-in-Package) featuring advanced miniature packaging technology and an ultra-small footprint designed to commit unique integration features for high volume and cost sensitive applications.

The ORG4475 module integrates LNA, SAW filter, TCXO, RTC crystal and RF shield with market-leading SiRFStarIV™ GPS processor.

The revolutionary SiRFStarIV™ architecture is optimized for how people really use their location-aware products: often indoors with periods of unobstructed sky view when moving from place to place.

Innovative GPS firmware can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and ephemeris data while consuming mere microwatts of battery power.

1.2 About OriginGPS

OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.

OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.

Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.

2. Description

OriginGPS has researched and enhanced the performance of standard GPS receivers in real life applications.
Research on key components results in module's higher sensitivity, faster position fix, better navigation stability and operation robustness under rapid environmental changes creating hard-to-achieve laboratory performance in heavy-duty environment.

2.1 Features

- Stand-alone operation
- OriginGPS Noise Free Zone System (NFZ™) technology
- Integrated LNA, SAW Filter, TCXO, RTC Crystal, RF Shield, Power Management Unit
- 50Ω antenna input
- Active or Passive antenna support
- GPS L1 (1575MHz) frequency, C/A code
- SBAS (WAAS, EGNOS, MSAS) and QZSS support
- 48 tracking channels
- High Sensitivity: -163dBm during tracking
- Short Time To First Fix (TTFF): < 1s under Hot Start conditions
- Low Power Consumption: < 9mW in ATP™ mode
- High Accuracy: < 2.5m CEP (50%)
- Update rate: 1Hz (default), 5Hz
- Autonomous A-GPS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- Predictive A-GPS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- Multipath Mitigation
- Cross-correlation Mitigation
- Indoor Tracking
- Active Jammer Detector and Remover
- Low power modes: ATP™, PTF™, APM™, SiRFAware™ MPM
- Almanac Based Positioning (ABP™)
- ARM7® 109MHz microprocessor system
- Selectable UART, SPI or I^2C host interface
- Programmable baud rate and messages rate
- 1PPS output
- Single voltage supply
- Ultra-small footprint: 5.6mm x 5.6mm
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Operating temperature range: -40^0C to 85^0C
- FCC and CE certified
- Pb-Free RoHS/REACH compliant

2.2 Architecture

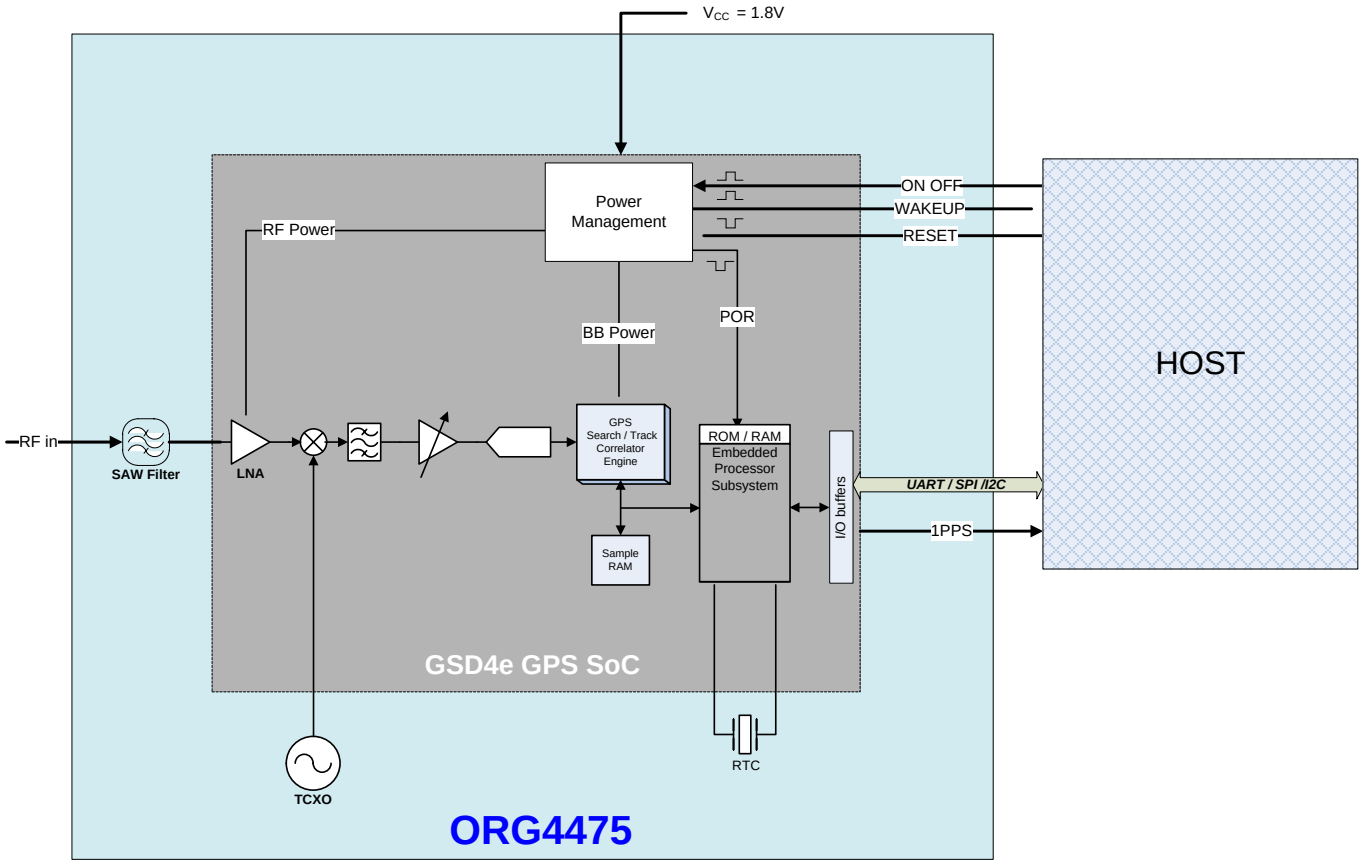

Figure 2-1: ORG4475 architecture

- **Band-Pass SAW (Surface Acoustic Wave) Filter**

  Band-pass SAW filter eliminates inter-modulated out-of-band signals that may corrupt GPS receiver performance.

- **LNA (Low Noise Amplifier)**

  The integrated LNA amplifies the GPS signal to meet RF down converter input threshold. Noise Figure optimized design was implemented to provide maximum sensitivity.

- **TCXO (Temperature Compensated Crystal Oscillator)**

  This highly stable 16.369 MHz oscillator controls the down conversion process in RF block of the GPS processor.
  Characteristics of this component are important factors in higher sensitivity, shorter TTFF and better navigation stability.

- **RTC (Real Time Clock) crystal**

  Tuning fork quartz crystal component with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the ORG4475 module.

- **RF Shield**

  RF enclosure avoids external interference to compromise sensitive circuitry inside the receiver. RF shield also blocks module's internal high frequency emissions from being radiated.

- **GSD4e IC**

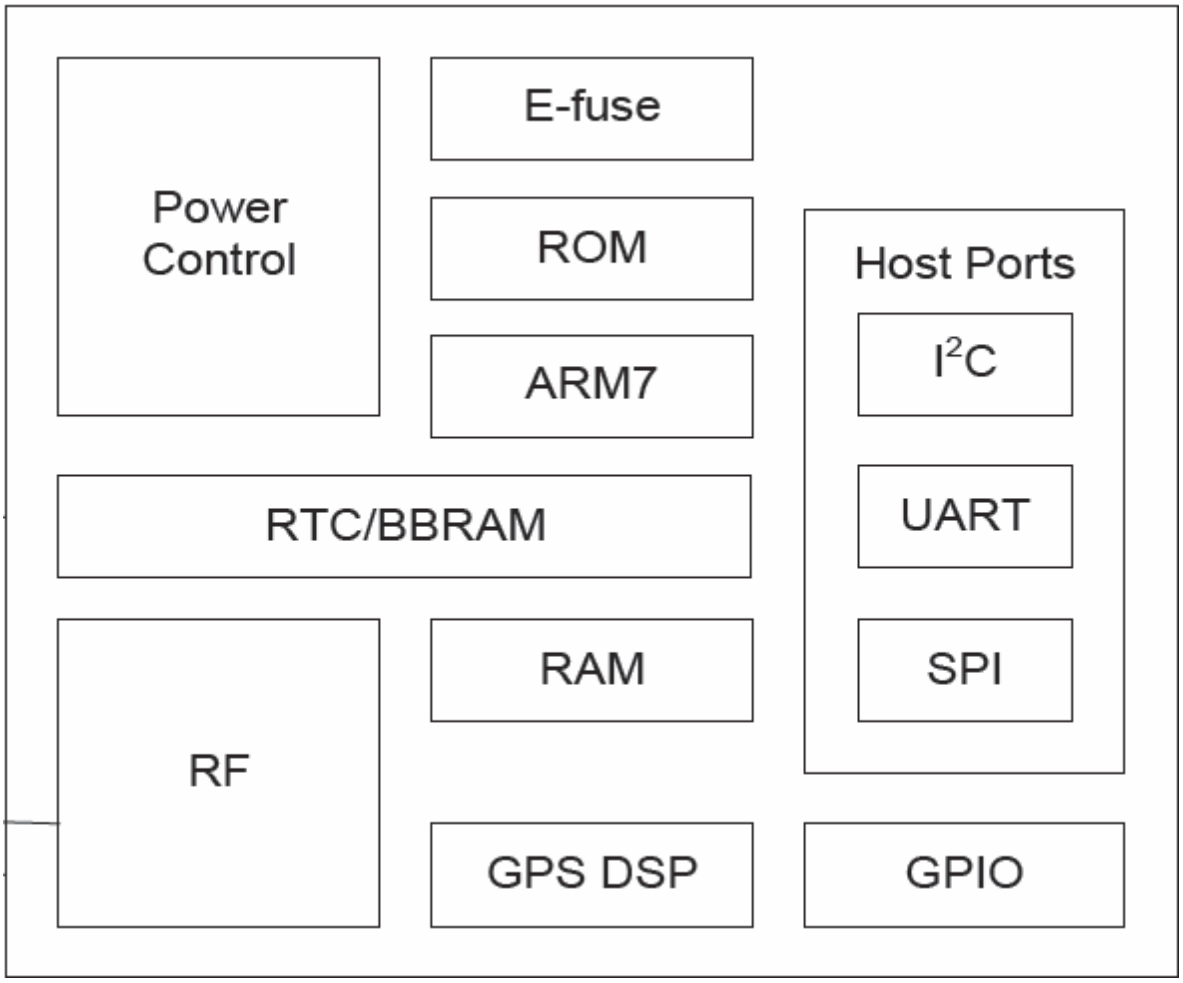

Figure 2-2: GSD4e functional block diagram

SiRFstarIV™ GSD4e is full System-On-Chip (SoC) built on a low-power RF CMOS single-die, incorporating the RF, the baseband, integrated navigation solution software, ARM7® processor. SiRFstarIV™ GSD4e SoC includes the following units:

- GPS RF core incorporating LNA, down converter, fractional-N synthesizer and ADC block with selectable 2 and 4-bit quantization
- GPS DSP core incorporating more than twice the clock speed and more than double the RAM capacity relative to predecessor - market benchmarking SiRFStarIII™ GPS processor
- ARM7® microprocessor system incorporating 109MHz CPU and interrupt controller
- ROM block as firmware storage
- RAM block for data cache
- RTC block
- UART block
- SPI block
- Power control block for internal voltage domains management

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings are stress ratings only.

Stresses exceeding Absolute Maximum Ratings may damage the device.

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		V_{CC}	-0.3	+2.2	V
RF Input Voltage		V_{RF}	-10	+10	V
I/O Voltage		V_{IO}	-0.3	+3.6	V
I/O Source/Sink Current		I_{IO}	-2	+2	mA
ESD Rating	I/O pads	$V_{IO(ESD)}$	-2	+2	kV
	RF input pad	$V_{RF(ESD)}$	ESD Sensitive		
RF Input Power	f_{IN} = 1560MHz÷1590MHz	P_{RF}	-	+10	dBm
	f_{IN} <1560MHz, >1590MHz		-	+30	dBm
Power Dissipation		P_D	-	200	mW
Storage Temperature		T_{ST}	-55	+125	^{0}C
Lead Temperature (10 sec. @ 1mm from case)		T_{LEAD}	-	+260	^{0}C

Table 3-1: Absolute maximum ratings

3.2 Recommended Operating Conditions

Functional operation above the Recommended Operating Conditions is not implied.
Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Parameter	Symbol	Mode / Pad	Test Conditions	Min	Typ	Max	Units
Power supply voltage	V_{CC}			+1.71	+1.80	+1.89	V
Power Supply Current	I_{CC}	Acquisition	-130dBm (Outdoor) $T_{AMB} = 25^0C$		33	43	mA
		Tracking		5		33	mA
		CPU only[1]			14		mA
		MPM™[2]			0.5		mA
		Standby[1]			90		µA
		Hibernate			12	20	µA
Input Voltage Low State	V_{IL}	GPIO		-0.4		+0.45	V
Input Voltage High State	V_{IH}			$0.70 \cdot V_{CC}$		+3.6	V
Output Voltage Low State	V_{OL}		I_{OL} = 2mA			+0.40	V
Output Voltage High State	V_{OH}		I_{OH} = -2mA	$0.75 \cdot V_{CC}$	V_{CC}-0.1		V
Input Capacitance	C_{IN}				5	8	pF
Internal Pull-up Resistor	R_{PU}			50	86	157	kΩ
Internal Pull-down Resistor	R_{PD}			51	91	180	kΩ
Input Leakage Current	$I_{IN(leak)}$		V_{IN} = 1.8V or 0V	-10		+10	µA
Output Leakage Current	$I_{OUT(leak)}$		V_{OUT} = 1.8V or 0V	-10		+10	µA
Input Impedance	Z_{IN}	RF Input	f_0 = 1575.5 MHz		50		Ω
Input Return Loss	RL_{IN}				-8		dB
Operating Temperature[3]	T_{AMB}			-40	+25	+85	^0C
Relative Humidity	RH		$-40^0C \leq T_{AMB} \leq +85^0C$	5		95	%

Table 3-2: Recommended operating conditions

Notes:
1. Transitional states of ATP™ low power mode
2. Average current during SiRFAware™ Micro Power Mode
3. Operation below -20^0C to -40^0C and above $+70^0C$ to $+85^0C$ is accepted, but TTFF may increase

4. Performance

4.1 Acquisition Times

TTFF (Time To First Fix) – is the period of time from the module's power-up till position estimation.

Hot Start

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.
During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

Warm Start

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.
In this state, position and time data are present and valid, but satellite ephemeris data validity has expired.

Cold Start

Cold Start acquisition trial occurs when satellite ephemeris data, position and time data are unknown.

Aided Start

Aided Start is a method of effectively reducing the TTFF by making every start Hot or Warm.

	TTFF	Test Condition	Signal Level
Hot Start	< 1s	Outdoor, Static	-130dBm
Aided Start	< 10s		
Warm Start	< 32s		
Cold Start	< 35s		
Signal Reacquisition	< 1s		

Table 4-1: Acquisition times

4.2 Sensitivity

Operation	Signal Level
Tracking	-163dBm
Navigation	-161dBm
Aided	-156dBm
Cold Start	-148dBm

Table 4-2: Sensitivity

4.3 Power Consumption

Operation	Power Consumption
Acquisition	75mW
Tracking	9 - 60mW
Hibernate	22µW

Table 4-3: Power consumption

4.4 Accuracy

		Method	Accuracy	Units	Test Conditions	Signal Level
Position	Horizontal	CEP (50%)	< 2.5	m	Outdoor, 24-hr static	-130dBm
			< 2	m		
		2dRMS (95%)	< 5	m		
			< 4	m		
	Vertical	VEP (50%)	< 4	m		
			< 3	m		
		2dRMS (95%)	<7.5	m		
			< 6	m		
Velocity	Horizontal	50%	< 0.01	m/s	Outdoor, 30 m/s	
Heading		50%	< 0.01	0		
Time		1 PPS	< 100	ns	Outdoor, 24-hr static	

Table 4-4: Accuracy

4.5 Dynamic Constrains

	MAXIMUM[1]	
Velocity <	515 m/s	1,000 knots
Acceleration <	4g	
Altitude <	18,288 m	60,000 ft.

Table 4-5: Dynamic constrains

Note:
1. Standard dynamic constrains according to regulatory limitations.

5. Power Management

5.1 Power States

Full Power state (Acquisition/Tracking)

The ORG4475 module stays in full power until a position solution is made and estimated to be reliable.
During the acquisition, processing is more intense than during tracking, thus consuming more power.

CPU Only state

This is the state when the RF and DSP sections are partially powered off.
The state is entered when the satellites measurements have been acquired but the navigation solution still needs to be computed.

Standby state

This is the state when the RF and DSP sections are completely powered off and baseband clock is stopped.

Hibernate state

In this state the RF, DSP and baseband sections are completely powered off leaving only the RTC and Battery-Backed RAM running.
The module will perform Hot Start if remain in Hibernate state less than 4 hours after valid position solution was acquired.

5.2 Power Saving Modes

The ORG4475 module has different power management modes - ATP™, APM™, PTF™ and SiRFAware™ Micro Power Mode (MPM) which are controlled by internal state machine.
These modes provide different levels of power saving with different degradation level of position accuracy.

Adaptive Trickle Power (ATP™)

Adaptive Trickle Power (ATP™) is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position.
In ATP™ mode the ORG4475 module is intelligently cycled between Full Power, CPU Only and Standby states to optimize low power operation.

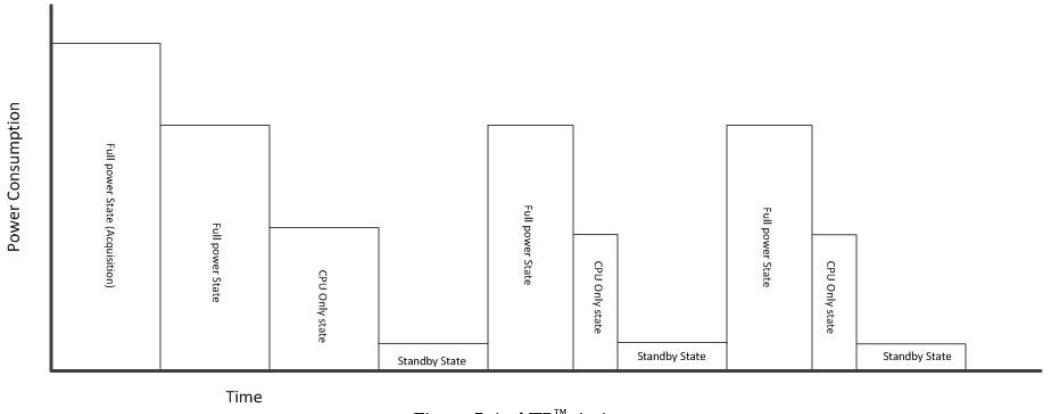

Figure 5-1: ATP™ timing

Push-to-Fix (PTF™)

Push-to-Fix (PTF™) is best suited for applications that require infrequent navigation solutions, optimizing battery life time.
In PTF™ mode the ORG4475 module is mostly in Hibernate state, drawing < 15µA of current, waking up for Ephemeris and Almanac refresh in fixed periods of time.
The PTF™ period is 30 minutes by default but can be anywhere between 10 seconds and 2 hours.
When the PTF mode is enabled the receiver will stay in Full Power state until the good navigation solution is computed.
When the application needs a position report it can toggle the ON_OFF pad to wake up the module.

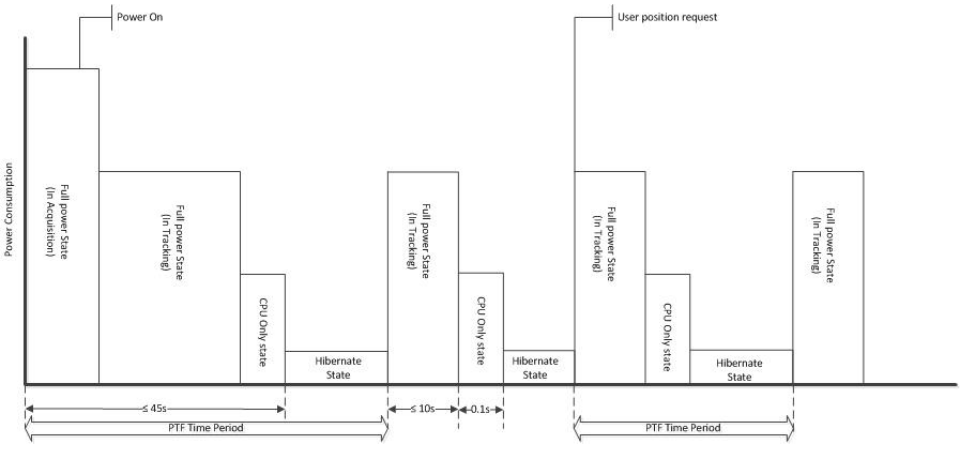

Figure 5-2: PTF™ timing

Advanced Power Management (APM™)

Advanced Power Management (APM™) is designed to give the user more options to configure the power management. The APM™ mode allows power savings while ensuring that the Quality of the Solution (QoS) in maintained when signals level drop.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.
The user may select between Duty Cycle Priority for more power saving and Time Between Fixes (TBF) priority with defined or undefined maximum horizontal error.
TBF range is from 10 to 180 sec. between fixes, Power Duty Cycle range is between 5 to 100%.
Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.

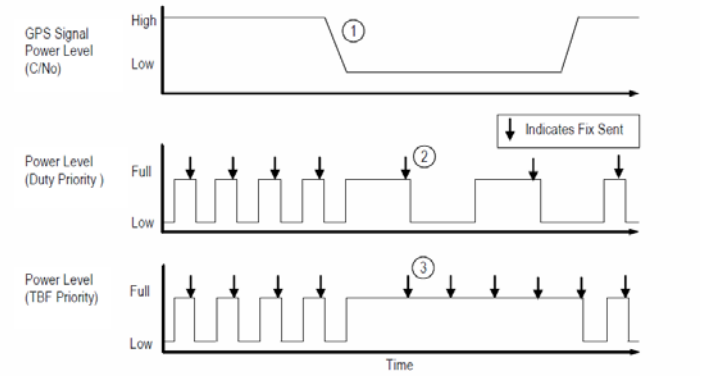

Figure 5-3: APM™ timing

1. GPS signal level drops (e.g. user walks indoors)
2. Lower signal results in longer ON time. To maintain Duty Cucle, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs, the module goes info Full Power state until signal levels improve.

SiRFAware™ Micro Power Mode (MPM)

While in SiRFAware™ MPM the ORG4475 module determines how much signal processing to do and how often to do it, so that the module is always able to do a fast hot start (TTFF < 2 s) on demand.
The ORG4475 module is configured to wake up (typically twice an hour) for 18-24 sec. to collect new Ephemeris data. Ephemeris data collection operation consumes the current equal to Full Power.
Additionally, the module will wake up once every 1 to 10 min. for 250ms to update internal navigation state and GPS time calibration. Capture/Update operation consumes about 200µA.
Rest of the time the receiver remains in Hibernate state.
The host toggles ON_OFF to wake-up the ORG4475 module.
After valid fix is available, the host can turn the module back into MPM by re-sending the command.
Average current consumption over long period during MPM is about 500µA.

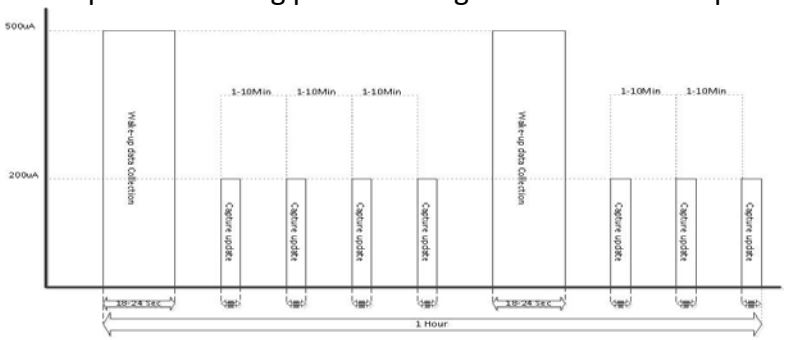

Figure 5-4: MPM™ timing

6. Extended Features

6.1 Almanac Based Positioning (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as a tradeoff with the accuracy. When no sufficient Ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites having their states derived from the Almanac data.
Data source for ABP™ may be either stored factory Almanac, broadcasted or pushed Almanac.

6.2 Active Jammer Remover

Jamming Remover is an embedded DSP block that detects, tracks and removes up to 8 Continuous Wave (CW) type signals of up to 80dB-Hz each.
Jamming Remover is effective only against continuous narrow band interference signals and covers GPS L1 1575Mhz frequency ±4MHz.

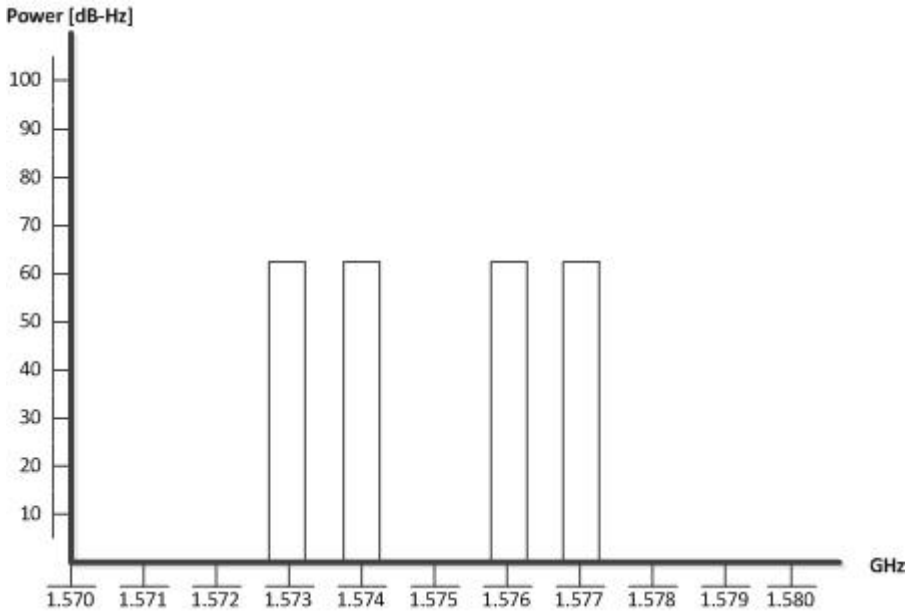

Figure 6-1: Active Jammer Detection frequency plot

6.3 Client Generated Extended Ephemeris (CGEE™)

The CGEE™ feature allows shorter TTFF by providing predicted (synthetic) ephemeris files created within a lost host system from previously received broadcast Ephemeris.
The prediction process requires good receipt of broadcast Ephemeris data for all satellites.
EE files created this way are good for up to 3 days and then expire.
The CGEE™ feature requires avoidance of power supply removal.
CGEE™ data files are stored and managed by host.

7. Interface

7.1 Pad Assignment

Pad	Name	Description	Direction	Full Power	Hibernate	Notes
1	GND	System Ground	Power			
2	WAKEUP	Power Status	Output	High	Low	1.8V compatible
3	$\overline{CTS}$	UART CTS / SPI CLK	Bi-directional	Low	Low	Internal pull-down
4	V_{CC}	System Power	Power			1.8V
5	$\overline{RESET}$	Asynchronous Reset	Input	High	High	Internal pull-up
6	$\overline{RTS}$	UART RTS / SPI nCS	Bi-dir.	High	High	Internal pull-up
7	RX	UART RX / SPI MOSI / I^2C SDA	Bi-dir.	High	Hi-Z	1.8 – 3.6V
8	GND	System Ground	Power			
9	1PPS	UTC Time Mark	Output	Low	Low	1.8V compatible
10	ON_OFF	Power State Control	Input	Low	Low	1.8 – 3.6V
11	NC	Not Connected				
12	GND	System Ground	Power			
13	NC	Not Connected				
14	TX	UART TX / SPI MISO / I^2C SCL	Output	High	Hi-Z	1.8V compatible
15	NC	Not Connected				
16	NC	Not Connected				
17	GND	System Ground	Power			
18	RF_IN	Antenna Signal Input	Input			
19	GND	System Ground	Power			

Table 7-1: ORG4475 pin-out

7.2 Connectivity

7.2.1. Power

It is recommended to keep the power supply on all the time in order to maintain the non-volatile RTC and RAM active for fastest possible TTFF.
When the V_{CC} is powered off settings are reset to factory default and the receiver performs Cold Start on next power up.

Vcc

The V_{CC} is 1.8V DC.
Typical I_{CC} current is 37mA during acquisition. Peak I_{CC} current is 60mA.
Typical I_{CC} current in Hibernate state is 12µA.
Voltage ripple below 50mV_{PP} allowed for frequency between 100KHz to 1MHz.
Voltage ripple below 15mV_{PP} allowed for frequency above 1MHz.
Higher voltage ripple may compromise the module performance.

Ground

Ground pad should be connected to host PCB Ground with shortest possible trace or via.

7.2.2. RF input

The antenna input impedance is 50Ω.
The module supports active or passive antenna.
In design with passive antenna attention should be paid on antenna layout.
Short trace with controlled impedance of 50Ω should conduct GPS signal from antenna to RF_IN pad.
In designs with active antenna DC bias voltage should be applied on RF_IN through bias-T.
DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.
In designs with active antenna net gain including conduction losses should not exceed 25dB.
In designs with external LNA, LNA enable input can be controlled by the ORG4475 WAKEUP output.

7.2.3. Host Control Interface

ON OFF input

The ON_OFF control input is used to switch the ORG4475 between different power states.

- If the module is in Hibernate state, an ON_OFF pulse will move to Full Power mode.
- If the module is in ATP™ mode, an ON_OFF pulse will move it to Full Power mode.
- If the module is in PTF™ mode, an ON_OFF pulse will initiate one PTF™ cycle.
- If the module is already in Full Power mode, an ON_OFF pulse will initiate orderly shutdown.

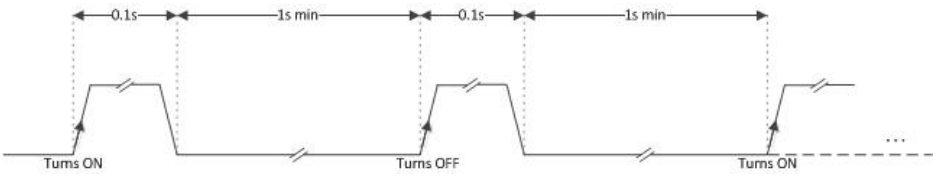

Figure 7-1: Recommended ON_OFF timing

ON_OFF pulse requires a rising edge and high logic level that persists for at least 100µs in order to be detected.
ON_OFF detector reset requires that ON_OFF asserted to low logic level for at least 100µs.
Recommended ON_OFF low-high-low pulse length is 100ms.
ON_OFF interrupts with less than 1 sec intervals are not recommended.
Multiple switch bounce pulses are recommended to be filtered out.
ON_OFF input is 3.6V tolerant. Pull-down resistor of 33kΩ-82kΩ is recommended.
Do not drive high permanently or pull-up this input.
Must be connected to host.

WAKEUP output

The WAKEUP pad is an output from the ORG4475 module, used to flag for power state.
A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.
In addition WAKEUP output can be used to control auxiliary devices.
Wakeup output is LVCMOS 1.8V compatible. Do not connect if not in use.

$\overline{\text{RESET}}$ input

The Power-on-Reset (POR) is generated internally in the ORG4475 module.
Additionally, manual reset option is available through $\overline{\text{RESET}}$ pad.
Resetting the module clears the RTC block and configuration settings become default.
$\overline{\text{RESET}}$ signal should be applied for at least 1µs.
$\overline{\text{RESET}}$ input is active low and has internal pull-up resistor of 86kΩ.
Do not drive this input high. Do not connect if not in use.

1PPS output

The pulse-per-second (PPS) output provides a pulse signal for timing purposes.
Pulse length (high state) is 200ms and it's rising edge is 100ns synchronized to UTC epoch.
The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal.
The exact time between the PPS and the UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible. Do not connect if not in use.

7.2.4. Host Data Interface

The ORG4475 module has 3 types of interface ports to connect to host: UART, SPI and I^2C.
All ports are multiplexed on a shared set of pads.
At system reset, the host port interface lines are disabled, so no conflict occurs.
Configuration straps on nCTS and nRTS are read by the module firmware during startup and define port type. 10kΩ resistor is recommended for external strap.

Port Type	nCTS	nRTS
UART	External pull-up	Internal pull-up
SPI (default)	Internal pull-down	Internal pull-up
I^2C	Internal pull-down	External pull-down

Table 7-2: ORG4475 host interface selection

UART

The module has a standard UART port:

- TX used for GPS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V to 3.6V.

Operation:

The UART performs bit-by-bit transmitting and receiving in 8-bit octets when module is active.
On the transmit side 1 start bit, 8 data bits and 2 stop bits followed by next character or idle.
Designers should treat computations of maximum message output capacity from the ORG4475 module with 11-bits per transmitted character.
On the receive side 1 start bit, 8 data bits, 1 stop bit or longer is accepted.

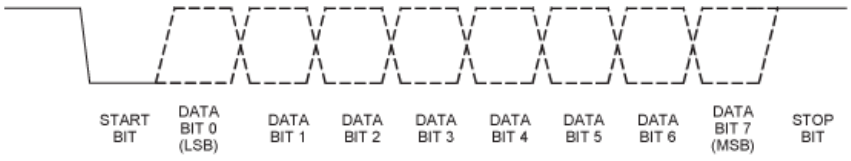

Figure 7-2: UART integrity

The default protocol is NMEA@4,800bps.
The configuration for baud rates and respective protocols can be changed by commands via NMEA or OSP™ protocols.

Baud Rate (bps)	Error (%)
4800	0.06
9600	0.00
19200	0.00
38400	0.07

Baud Rate (bps)	Error (%)
115200	0.24
230400	1.04
460800	0.60
921600	2.40

Table 7-3: UART baud rate tolerance

Because UART transmission is asynchronous and sampled by the receiver, both sides require closely match bit-rate clocks, and that data bit waveform and timing distortion at the receiver should be limited.

Maximum allowed clock rate difference between the ORG4475 and host is 2.0% overall.
Maximum bit-edge distortion ≤ 5% bit length. Maximum bit jitter ≤ 5% bit length.

SPI

The SPI (Serial to Peripheral Interface) is a master/slave synchronous serial bus that consists of 4 signals:

- Serial Clock (SCK) from master to slave.
- Serial Data Out (also called Master Out Slave In or MOSI) from master.
- Serial Data In (also called Master In Slave Out or MISO) from slave.
- Chip Select (CS) from master.

The host interface SPI of the ORG4475 module is a slave mode SPI.
The four SPI pads are RX (MOSI), TX (MISO), nRTS(nCS) and nCTS(SCK).
Output logic high voltage level is LVCMOS 1.8V compatible. Inputs are 3.6V tolerant.
The host interface SPI features are:

- TX and RX each have independent 1024 byte FIFO buffers.
- RX and TX have independent, software specified two byte idle patterns of '0xA7 0xB4'.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Supports a maximum clock of 6.8MHz.
- Default GPS data output format is NMEA standard.

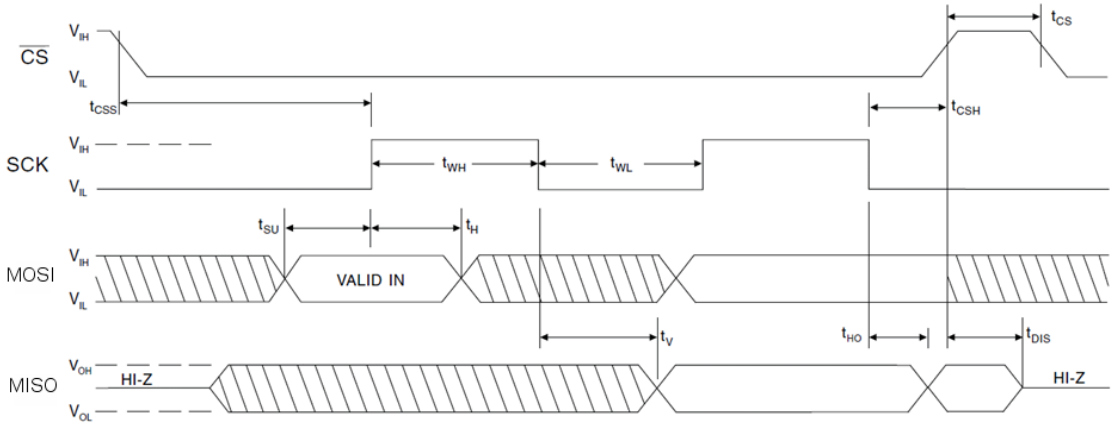

Figure 7-3: SPI timing

Symbol	Parameter	Min	Max	Units
t_{CLK}	SCK Time Period	140		ns
t_{CSS}	nCS Setup Time	0.5	1	t_{CLK}
t_{CS}	nCS High Time	1		t_{CLK}
t_{WH}	SCK High Time	0.5		t_{CLK}
t_{WL}	SCK Low Time	0.5		t_{CLK}
t_{CSH}	nCS Hold Time	0.5	1	t_{CLK}
t_{SU}	Data In Setup Time	0.5		t_{CLK}
t_H	Data In Hold Time	0.5		t_{CLK}
t_V	Output Valid	0.5		t_{CLK}
t_{HO}	Output Hold Time	0.5		t_{CLK}
t_{DIS}	Output Disable Time		0.5	t_{CLK}

Table 7-4: SPI timing

Operation:

The SPI performs bit-by-bit transmitting and receiving at the same time whenever nCS is asserted and SCK is active. In order to communicate properly with SPI device, the protocol must be agreed – specifically- SPI mode and an idle byte pattern.

Among 4 SPI modes of the clock polarity (CPOL) and clock phase (CPHA) only SPI Mode 1 <CPOL="0", CPHA ="1"> is currently supported:

- At CPOL="0" the base value of the clock is zero.
- For CPHA="1" data is read on the clock's falling edge and data is changed on a rising edge.

It takes about 100ms from power up for the module SPI drivers to get initialized.

The slave has no way of forcing data to the master to indicate it is ready for transmission - the master must poll the client periodically.

Since the specified idle 2-byte pattern for both receive and transmit is '0xA7 0xB4', the master can transmit this idle pattern into the slave repeatedly. If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate.

On the module receive side, the host is expected to transmit idle pattern when it is querying the module's transmit buffer. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the module hardware does not place most idle pattern bytes in its RX FIFO. Most messaging can be serviced with polling. The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing.

On the module transmit side the intent is to fill the FIFO only when it is disabled and empty. In this condition, the module's SPI driver software loads as many queued messages as can completely fit in the FIFO. Then the FIFO is enabled.

The host is required to poll messages until idle pattern bytes are detected.

At this point the module's FIFO is empty and disabled, allowing the module's SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

Notes:

For SPI communication, read and write operations both require data being sent to the Slave SPI (idle bytes for reads and message data for writes). Any time data is sent to the module via the SPI bus, the Slave SPI of the module will send an equal amount of data back to the host. These bytes must be buffered either in hardware or software, and it is up to the host to determine if the bytes received may be safely discarded (idle bytes), or should be passed on to the application handling GPS communication. Failure to properly handle data received from the SPI slave can result in corrupted GPS messages.

The external SPI master may send idle bytes and complete messages in a single transmission, provided that idle bytes shall not be inserted inside of a message.

The idle byte pattern and repeat count prevents the problem of messages lost due to normal occurrence of idle byte patterns within message data with high probability.

The external SPI master shall not send partial messages.

All transmissions from the SPI master shall be in multiples of 8 bits.

The external SPI master shall transmit the idle byte pattern when reading the SPI slave's transmit buffer when the master has no message data to transmit.

The SPI slave shall be serviced at a rate that will keep the TX FIFO empty.

I²C

I²C is a low- to medium-data-rate master/slave communication bus.
Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus. At that time, any device addressed is considered a slave.
The physical layer of I²C bus is a simple handshaking protocol that relies upon open collector outputs on the bus devices and the device driving or releasing the bus lines, so a pull-up resistor is needed on each wire of the bus.
I²C bus is a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
Serial 8-bit oriented bi-directional data transfers can be made at up to 100kbps in the Standard-mode of I²C bus and up to 400kbps in the Fast-mode.
The Host Interface I²C features are:

- Multi-Master I²C mode is supported by default.
- Individual transmit and receive FIFO length of 64 bytes.
- The default I²C address values are:
  - RX: 0x60
  - TX: 0x62
- Operation speed up to 400kbps.
- SCL and SDA require external pull-up resistors of 2.2kΩ (typ.).

Operation:

The operation of the I²C with a master transmit and slave receive mimics a UART operation, where both the module and the host can independently freely transmit.
It is possible to enable the master transmit and slave receive at the same time, as the I²C bus allows for contention resolution between the module and the host vying for the bus.
Figure 7-4 shows typical data transfers on the I²C bus.

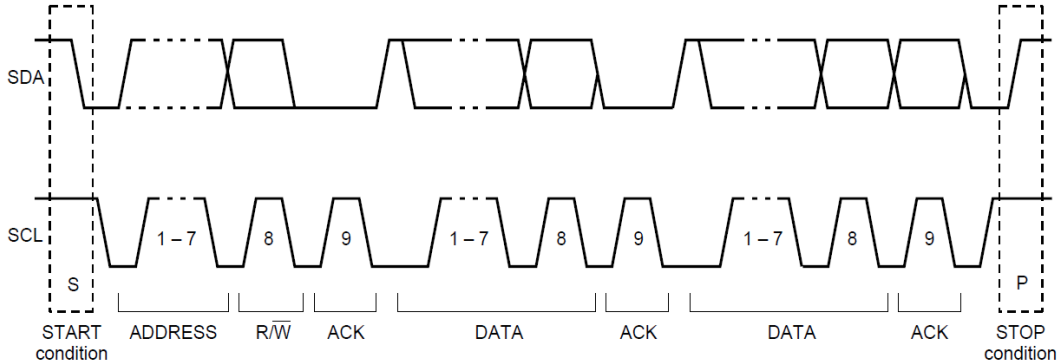

Figure 7-4: I²C integrity

The master supplies the clock; it initiates and terminates transactions and the intended slave (based upon the address provided by the master) acknowledges the master by driving or releasing the bus.
The slave cannot terminate the transaction but can indicate a desire to by a “NACK” or not-acknowledge.

I²C specification defines unique situations as START (S) and STOP (P) conditions.
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.
START and STOP conditions are always generated by the master.
Every byte put on the SDA line must be 8-bits long.
The number of bytes can be transmitted per transfer is unrestricted.
Each byte is followed by an acknowledge bit.
Data is transferred with the Most Significant Bit (MSB) first. In most cases, data transfer with acknowledge is obligatory. The acknowledge–related clock pulse is generated by the master.
The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.
The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.
Set-up and hold times must be taken into account.
All data transfers of I²C specification should follow the format.
After the START condition (S), a slave address should be sent first.
This address is 7 bits long followed by an 8-th bit which is a data direction bit (R/nW) – logical 0 indicates a transmission (WRITE), logical 1 indicates a request for data (READ).
After the slave address byte is sent, master can continue its data transfer by writing or reading data byte as defined format.
The data transfer is always terminated by a STOP condition generated by the master.

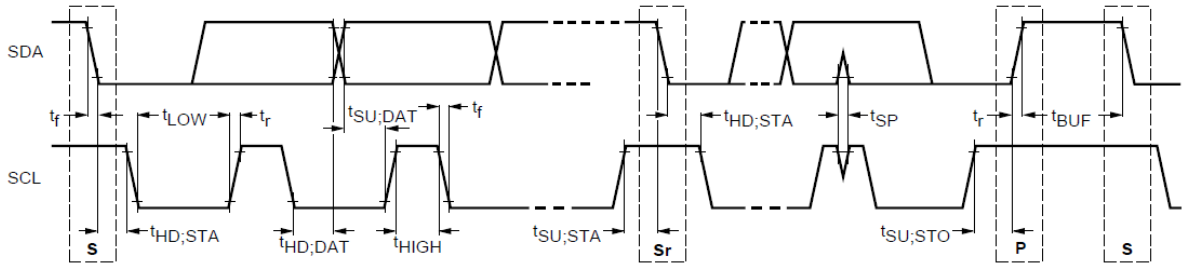

Figure 7-5: I²C timing

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL frequency	100	400	kHz
$t_{HD;STA}$	Hold Time for START condition	0.6		µs
t_{LOW}	Low Time of SCL	1.3		µs
t_{HIGH}	High Time of SCL	0.6		µs
$t_{SU;STA}$	Setup Time for START condition	0.6		µs
$t_{HD;DAT}$	Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Setup Time	0.1		µs
t_r	Rise Time of SDA and SCL		0.3	µs
t_f	Fall Time of SDA and SCL		0.3	µs
$t_{SU;STO}$	Setup Time for STOP condition	0.6		µs
t_{BUF}	Bus Free Time between START and STOP	1.3		µs
C_L	Capacitive Load of SDA and SCL		400	pF
V_{nL}	Noise Margin at the low logic level		$0.1 \cdot V_{CC}$	V
V_{nH}	Noise Margin at the high logic level		$0.2 \cdot V_{CC}$	V

Table 7-5: I²C timing

7.3 Typical Application Circuit

7.3.1. Minimal Schematics

UART Host Interface

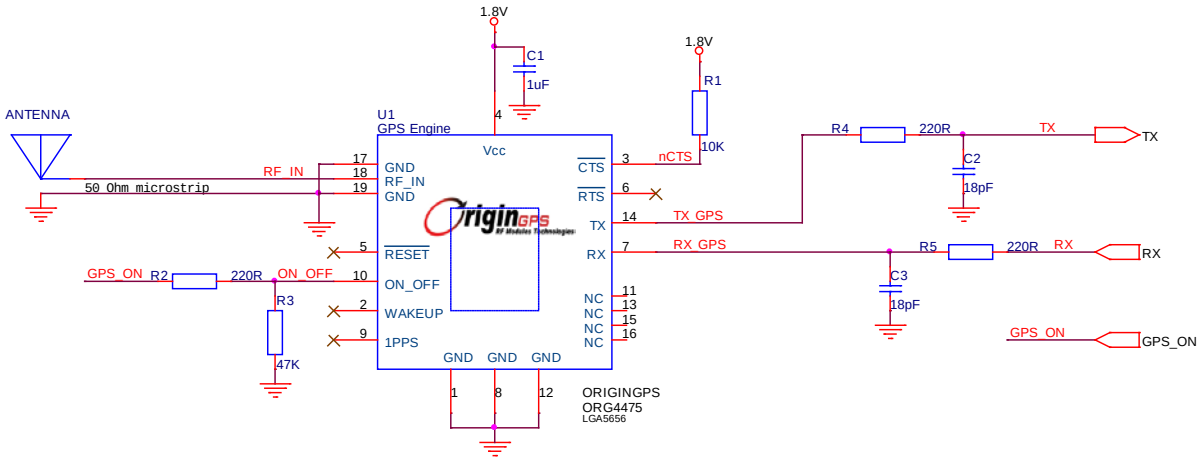

Figure 7-6: UART interface circuit

SPI Host Interface

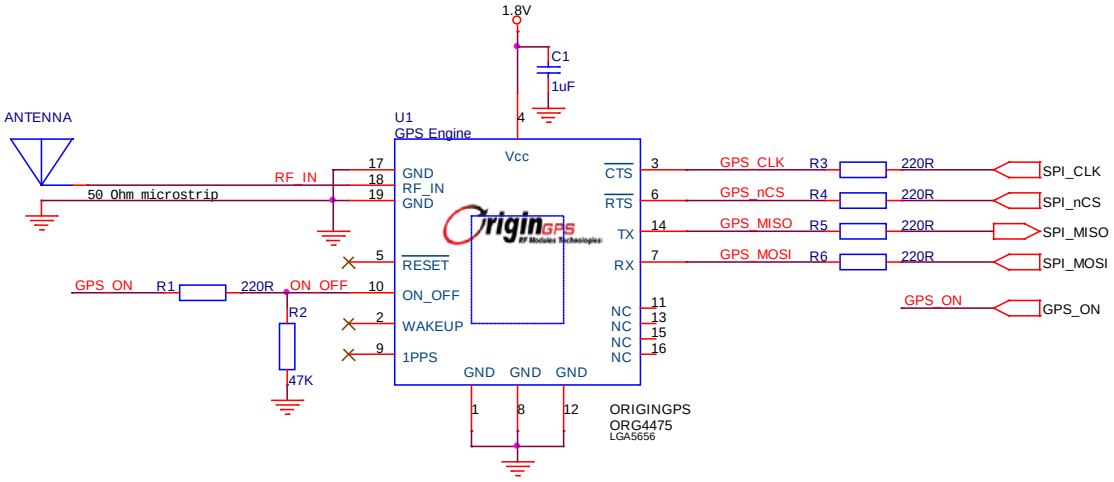

Figure 7-7: SPI interface circuit

I²C Host Interface

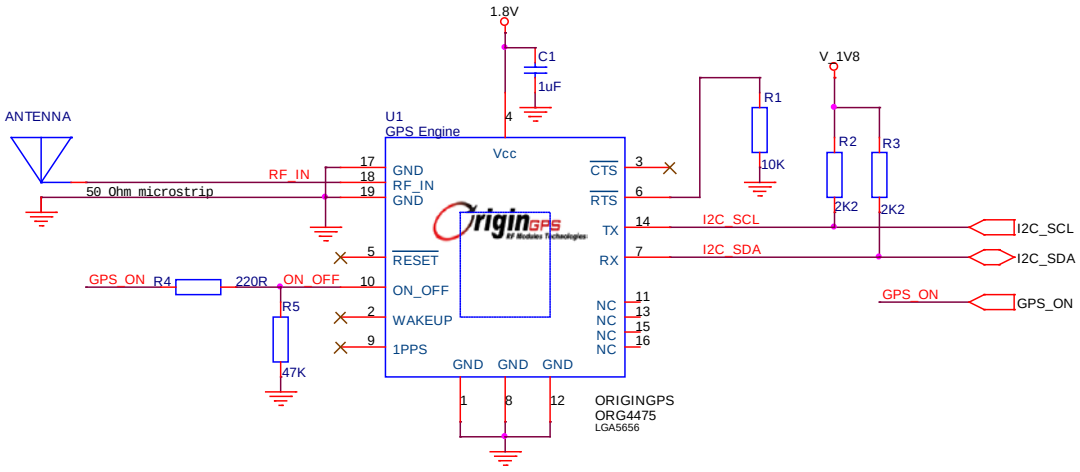

Figure 7-8: I²C interface circuit

7.3.2. Extended Schematics

Active Antenna, Voltage Regulator, Level Shifter

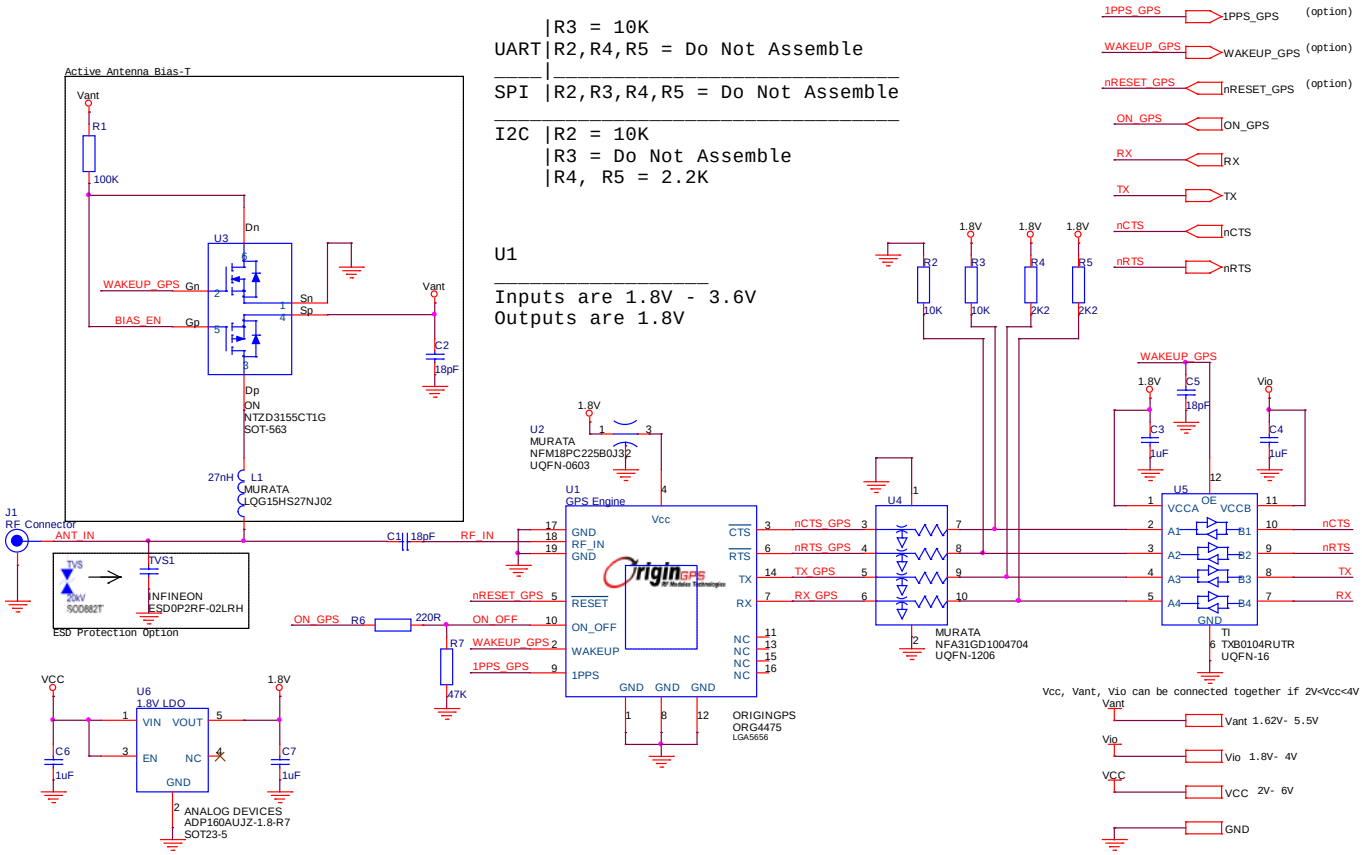

Figure 7-9: Active antenna circuit

Low Noise Amplifier, Voltage Regulator, Level Shifter

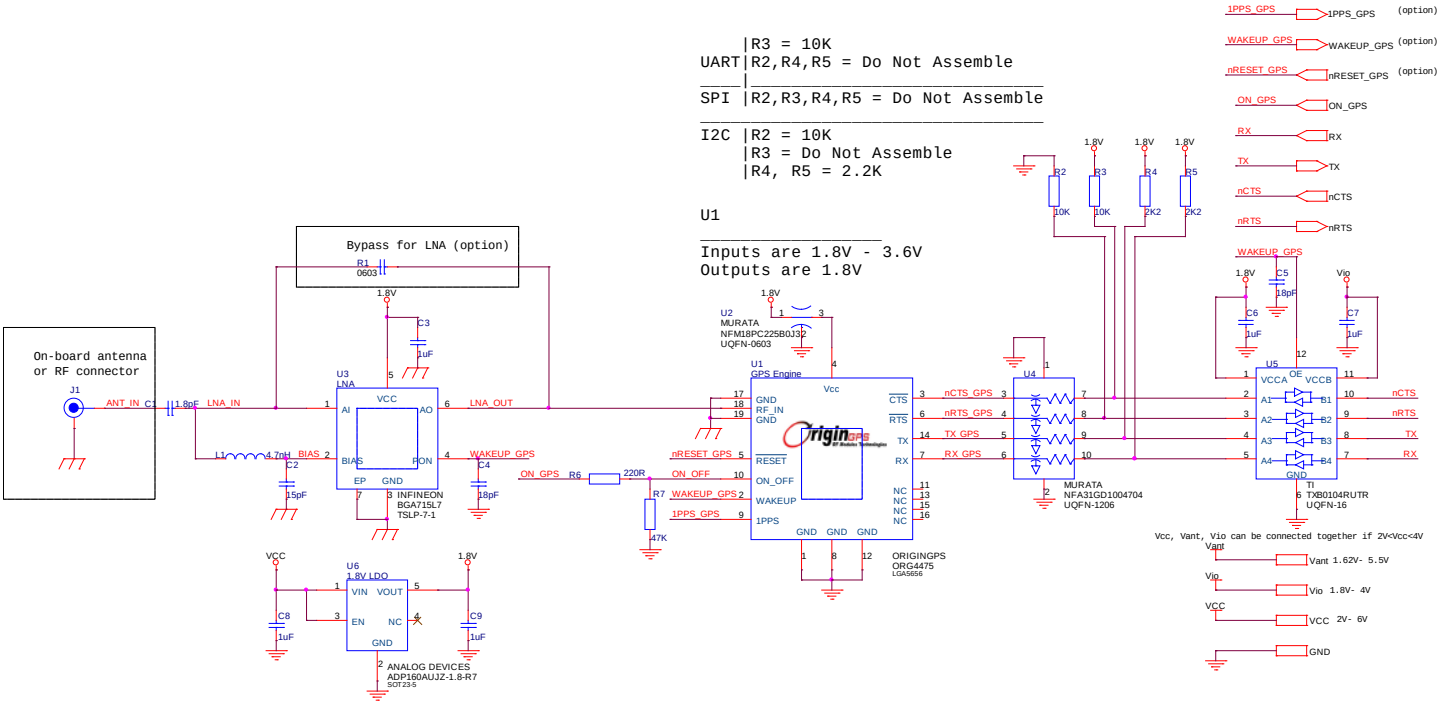

Figure 7-10: LNA circuit

8. PCB Layout

8.1 Footprint

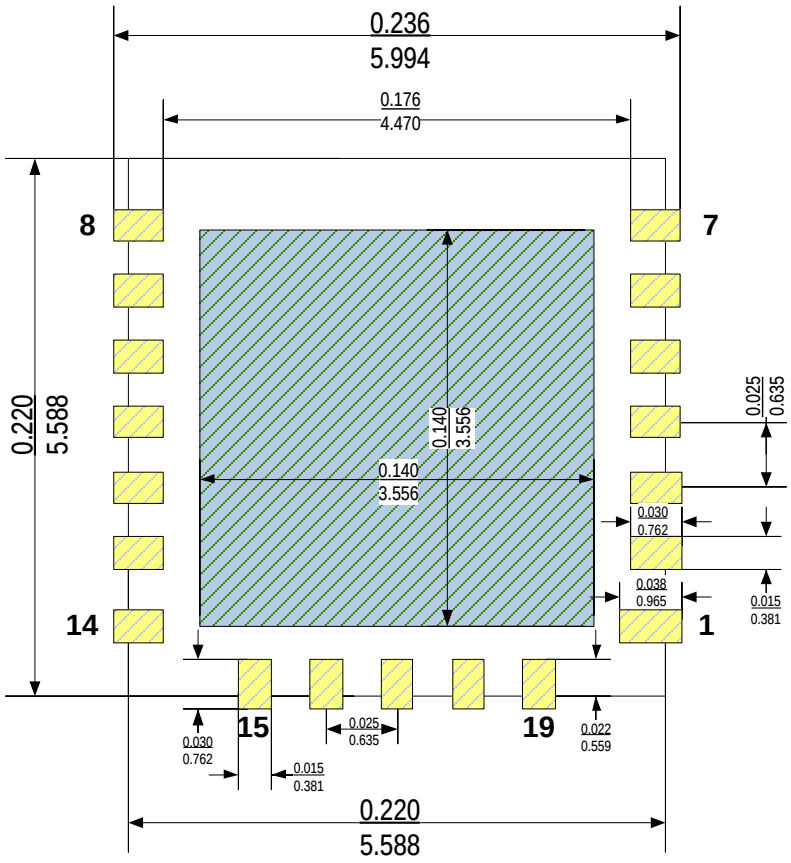

Figure 8-1: Footprint

Ground pad at the middle should be connected to main Ground plane by multiple vias.
Ground pad at the middle should be solder masked.
Silk print of module's outline on host PCB is highly recommended for SMT process.

8.2 RF Input trace

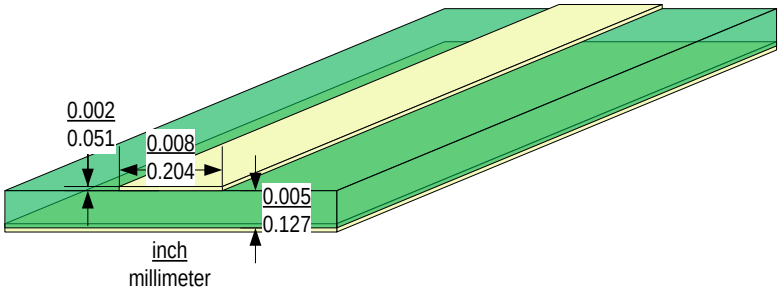

Figure 8-2: Typical Microstrip PCB trace on FR4 substrate

8.3 PCB stack up

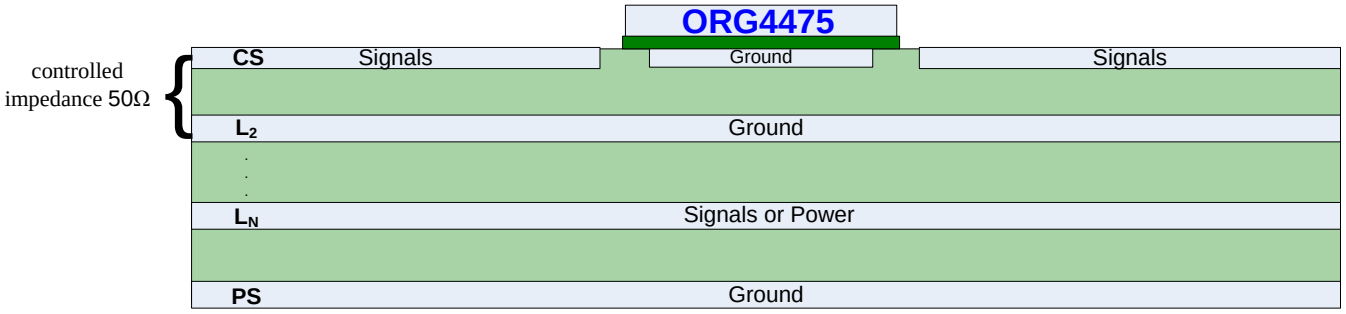

Figure 8-3: Typical PCB stack up

8.4 Design restrictions

Keep out of signal or switching power traces and vias under the ORG4475 module.
Signal traces to/from the ORG4475 module should have minimum length.
Recommended distance from adjacent active components is 3mm. In case of adjacent high speed components, like CPU or memory, high frequency components, like transmitters, clock resonators or oscillators, metal planes, like LCD or battery enclosures, please contact OriginGPS for more precise, application specific recommendations.

9. Operation

When power is first applied, the ORG4475 module goes into a Hibernate state while integrated RTC starts and internal FSM sequences though to "Ready-to-Start" state.
While in "Ready-to-Start" state, the module awaits a pulse to the ON_OFF input.
The host is not required to control $\overline{\text{RESET}}$ since module's internal voltage supervisor detects an application of power.

9.1 Starting the module

A pulse on the ON_OFF input will command the module to start.
Since integrated RTC startup times are variable, detection of when the module is ready to accept an ON_OFF pulse requires the host to either wait for a fixed interval of 1 sec., or to monitor a pulse on module WAKEUP output that indicates FSM "Ready-to-Start".
Optionally, a pulse on the ON_OFF input can be asserted every second until the module starts by indicating logic high level on WAKEUP output.

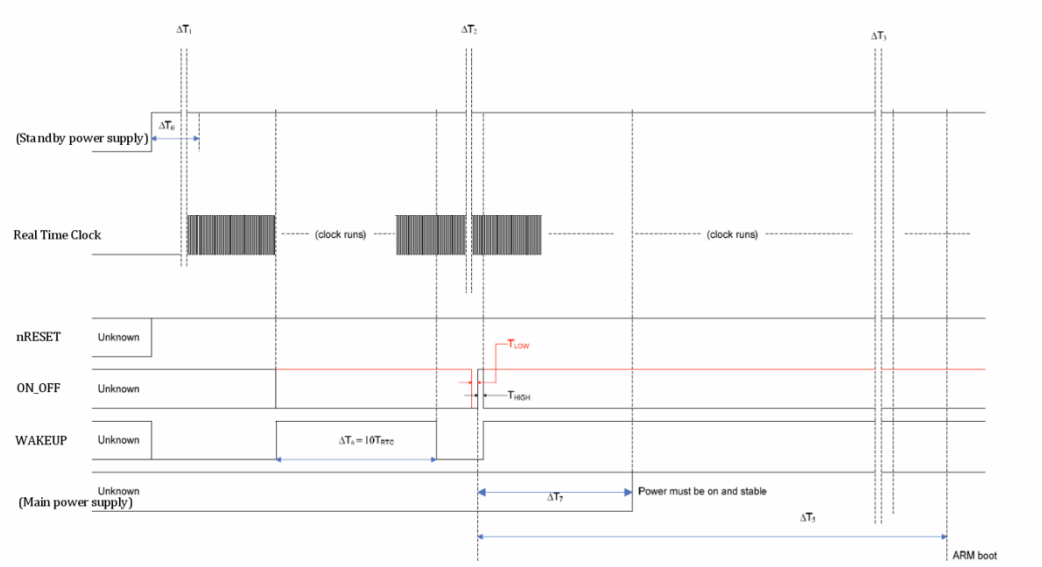

Figure 9-1: Startup timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{RTC}	RTC frequency	25^0C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC tick	25^0C		30.5176		µs
ΔT_1	RTC startup time			300		ms
ΔT_0	Power stabilization		$6 \cdot t_{RTC}+\Delta T_1$	$7 \cdot t_{RTC}+\Delta T_1$	$8 \cdot t_{RTC}+\Delta T_1$	µs
ΔT_6	WAKEUP pulse	RTC running		10		t_{RTC}
ΔT_{LOW}	ON_OFF low		3			t_{RTC}
ΔT_{HIGH}	ON_OFF high		3			t_{RTC}
ΔT_3	Startup sequencing	After ON_OFF		1024		t_{RTC}
-	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT_5	ON_OFF to ARM start	After ON_OFF		2130		t_{RTC}
ΔT_7	Main power source start[1]	WAKEUP high	0	30	300	t_{RTC}

Table 9-2: Startup timing

Note: When power provided through dual supply.
Low quescent current power source (LDO) for Hibernate state, and high efficiency source (DC-DC) for Full Power state.
The main power supply should be able to provide current for Full Power state within 1ms after WAKEUP is high.

9.2 Verifying the module has started

The ORG4475 module WAKEUP output will go logic high indicating the GPS processor has started. System activity indication depends upon the serial interface chosen.

UART:

- When active, the module will output NMEA messages at the 4800bps.
- The first message to come out of the module is the "OK_TO_SEND" - '$PSRF150,1*3E'.

SPI:

- Since the module is SPI slave, there is no possible indication of system "ready" through SPI interface.
- The host must initiate SPI connection approximately 1 sec. after WAKEUP output goes high.
- The first message to come out of the module is the "OK_TO_SEND" - '$PSRF150,1*3E'.

I^2C:

- In Multi-Master mode with no bus contention - the module will spontaneously send messages at the speed and message types selected.
- In Multi-Master mode with bus contention - the module will send messages after the I^2C bus contention resolution process allows it to send.

9.3 Shutting down the module

Transferring the ORG4475 module into Hibernate state can be initiated in two ways:

- By a pulse on the ON_OFF input when the module in Full Power state.
- By serial message MID205 (OSP™) or $PSRF117 (NMEA).

Last message before Hibernate state is '$PSRF150,0*3F'.

The orderly shutdown may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls.

10.Software Functions

The module supports NMEA protocol and One Socket Protocol (OSP™).

10.1 NMEA

NMEA is generic ASCII protocol used by general purpose GNSS receivers.

NMEA Output Messages

Message	Description
$GPGGA	Time, position and fix type data
$GPGLL[1]	Latitude, longitude, UTC time of position fix and status
$GPGSA	GPS receiver operating mode, satellites used in the position solution and DOP values
$GPGSV	The number of GPS satellites in view, satellite ID, elevation, azimuth and SNR values
$GPRMC	Time, date, position, course and speed data
$GPVTG[1]	Course and speed information relative to the ground
$GPZDA[1]	1PPS timing message
$PSRF150	OK to send data to the module
$PSRF155	Extended Ephemeris Proprietary Message
$PSRF156,0x20	ECLM ACK/NACK
$PSRF156,0x21	ECLM EE Get Age response
$PSRF156,0x22	ECLM Get SGEE Age response
$PSRF156,0x23	ECLM Download Initiate Request
$PSRF156,0x24	ECLM Erase Storage File
$PSRF156,0x25	ECLM Update File Content
$PSRF156,0x26	ECLM Request File Content

Table 10-1: NMEA protocol output messages

Note:

1. Not transmitted by default, can be enabled by $PSRF103 command

NMEA Input Messages

Message ID	Message	Description
$PSRF100	Set Serial Port	Set UART parameters and protocol
$PSRF101	Navigation Initialization	Parameters required for start using X/Y/Z
$PSRF103	Query/Rate Control	Query standard NMEA message and/or set output rate
$PSRF104	LLA Navigation Initialization	Parameters required for start using Lat/Lon/Alt
$PSRF105	Development Data On/Off	Development Data messages On/Off
$PSRF106	Select Datum	Selection of an alternative map datum
$PSRF107	Extended ephemeris proprietary message	
$PSRF108	Extended ephemeris proprietary message	
$PSRF110	Extended ephemeris debug	
$PSRF114,0x16	ECLM start download	
$PSRF114,0x17	ECLM file size	
$PSRF114,0x18	ECLM packet data	
$PSRF114,0x19	ECLM Get EE Age	
$PSRF114,0x1A	ECLM Get SGEE Age	
$PSRF114,0x1B	ECLM Host File Content	
$PSRF114,0x1C	ECLM Host ACK/NACK	
$PSRF117	System Turn Off	
$PSRF120	Storage Configuration Setting	

Table 10-2: NMEA protocol input messages

10.2 OSP™

OSP™ is a proprietary extension to SiRF Binary Standard protocol used by SiRF GPS processors.

OSP Binary Output Messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x 02	2	Measured Navigation Data			
0 x 03	3	True Tracker Data			
0 x 04	4	Measured Tracking Data			
0 x 06	6	SW Version			
0 x 07	7	Clock Status			
0 x 08	8	50 BPS Subframe Data			
0 x 09	9	Throughput			
0 x 0A	10	Error ID			
0 x 0B	11	Command Acknowledgement			
0 x 0C	12	Command No Acknowledgement			
0 x 0D	13	Visible List			
0 x 0E	14	Almanac Data			
0 x 0F	15	Ephemeris Data			
0 x 10	16	Test Mode 1			
0 x 12	18	Ok To Send			
0 x 13	19	Navigation Parameters			
0 x 14	20	Test Mode 2			
0 x 1B	27	DGPS Status			
0 x 1C	28	Nav. Lib. Measurement Data			
0 x 1E	30	Nav. Lib. SV State Data			
0 x 1F	31	Nav. Lib. Initialization Data			
0 x FF	255	Development Data			

Table 10-3: OSP binary output messages

OSP Binary Input Messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x 35	53	Advanced Power Management			
0 x 80	128	Initialize Data Source			
0 x 81	129	Switch to NMEA Protocol			
0 x 82	130	Set Almanac (upload)			
0 x 84	132	Software Version (Poll)			
0 x 86	134	Set Main Serial Port			
0 x 87	135	Switch Protocol			
0 x 88	136	Mode Control			
0 x 89	137	DOP Mask			
0 x 8A	138	MID_SET_DGPS_MODE			
0 x 8B	139	Elevation Mask			
0 x 8C	140	Power Mask			
0 x 8D	141	Editing Residual			
0 x 8E	142	Steady-State Detection			
0 x 8F	143	Static Navigation			
0 x 90	144	Poll Clock Status			
0 x 92	146	Poll Almanac			
0 x 93	147	Poll Ephemeris			
0 x 95	149	Set Ephemeris (upload)			
0 x 96	150	Switch Operating Mode			
0 x 97	151	Set Trickle Power Parameters			
0 x 98	152	Poll Navigation Parameters			
0 x A5	165	Set UART Configuration			
0 x A6	166	Set Message Rate			
0 x A7	167	Low Power Acquisition Parameters			
0 x A8	168	MID_POLL_CMD_PARAM			
0 x A9	169	Set Datum			
0 x AA	170	Set SBAS Parameters			
0 x AC	172	MID_DrIn	0 x 01	1	Set DrNavInit
			0 x 02	2	Set DrNavMode
			0 x 03	3	Set GyrFactCal
			0 x 04	4	Set DrSensParam
			0 x 05	5	Poll DrValid
			0 x 06	6	Poll GyrFactCal
			0 x 07	7	Poll DrSensParam
			0 x 13	19	DR Debug Information
0 x AF	175	Send Command String			
0 x B2	178	SIRF_MSG_SSB_TRACKER_IC	0 x 14	20	Patch Storage Control
			0 x 22	34	Patch Memory Load Request
			0 x 26	38	Patch Memory Exit Request
			0 x 28	40	Patch Memory Start Request
			0 x 90	144	Patch Manager Prompt
			0 x 91	145	Patch Manager Ack.
0 x CD	205	Set Generic Software Control	0 x 10	16	Software Commanded OFF
0 x D1	209	MID_QUERY_REQ			
0 x D2	210	MID_POS_REQ			

Table 10-4: OSP binary input messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x D3	211	MID_SET_AIDING	0 x 01	1	SET_IONO
			0 x 02	2	SET_EPH_CLOCK
			0 x 03	3	SET_ALM
			0 x 04	4	SET_ACQ_ASSIST
			0 x 05	5	SET_RT_INTEG
			0 x 06	6	SET_UTC_MODEL
			0 x 07	7	SET_GPS_TOW_ASSIST
			0 x 08	8	SET_AUX_NAV
			0 x 09	9	SET_AIDING_AVAIL
0 x D4	212	MID_STATUS_REQ	0 x 01	1	EPH_REQ
			0 x 02	2	ALM_REQ
			0 x 03	3	B_EPH_REQ
			0 x 04	4	TIME_FREQ_APPROX_POS_REQ
			0 x 05	5	CH_LOAD_REQ
			0 x 06	6	CLIENT_STATUS_REQ
			0 x 07	7	OSP_REV_REQ
			0 x 08	8	SERIAL_SETTINGS_REQ
0 x D5	213	MID_SESSION_CONTROL_REQ	0 x 01	1	SESSION_OPEN_REQ
			0 x 02	2	SESSION_CLOSE_REQ
0 x D6	214	MID_HW_CONFIG_RESP			
0xD7	215	MID_AIDING_RESP	0 x 01	1	APPROX_MS_POS_RESP
			0 x 02	2	TIME_TX_RESP
			0 x 03	3	FREQ_TX_RESP
			0 x 04	4	SET_NBA_SF1_2_3
			0 x 05	5	SET_NBA_SF4_5
0xD8	216	MID_MSG_ACK_IN	0 x 01	1	ACK_NACK_ERROR
			0 x 02	2	REJECT
0xD9	217		0 x 01	1	SENSOR_ON_OFF
0xDA	218	MID_PWR_MODE_REQ	0 x 00	0	FP_MODE_REQ
			0 x 01	1	APM_REQ
			0 x 02	2	MPM_REQ
			0 x 03	3	TP_REQ
			0 x 04	4	PTF_REQ
0xDB	219	MID_HW_CTRL_IN	0 x 01	1	VCTCXO
			0 x 02	2	ON_OFF_SIG_CONFIG
0xDC	220	MID_CW_CONTROLLER_REQ	0 x 01	1	CONFIG
			0 x 02	2	EVENT_REG
			0 x 03	3	COMMAND_SCAN
			0 x 04	4	CUSTOM_MON_CONFIG
			0 x 05	5	FFT_NOTCH_SETUP
0xE1	225	MID_SiRFOutput	0 x 06	6	STATISTICS
			0 x 07	7	Statistics with Aiding

Table 10-4: OSP binary input messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0xE8	232	MID_EE_INPUT	0 x 01	1	SSB_EE_SEA_PROVIDE_EPH
			0 x 02	2	SSB_EE_POLL_STATE
			0 x 10	16	SSB_EE_FILE_DOWNLOAD
			0 x 11	17	SSB_EE_QUERY_AGE
			0 x 12	18	SSB_EE_FILE_PART
			0 x 13	19	SSB_EE_DOWNLOAD_TCP
			0 x 14	20	SSB_EE_SET_EPHEMERIS
			0 x 15	21	SSB_EE_FILE_STATUS
			0 x 16	22	ECLM Start Download
			0 x 17	23	ECLM File Size
			0 x 18	24	ECLM Packet Data
			0 x 19	25	Get EE Age
			0 x 1A	26	Get SGEE Age
			0 x 1B	27	ECLM Host File Content
			0 x 1C	28	ECLM Host ACK/NACK
			0 x 1D	29	ECLM Get NVM Header
			0 x FD	253	EE_STORAGE_CONTROL
			0 x FE	254	SSB_EE_DISABLE_EE_SECS

Table 10-4: OSP binary input messages

11.Handling Information

11.1 Product Packaging and Delivery

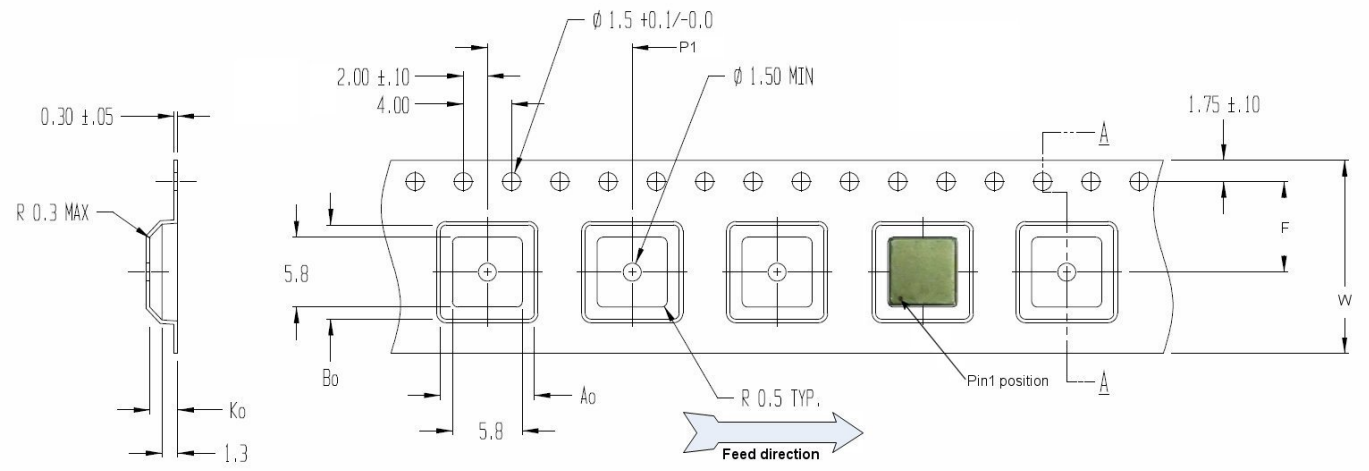

Figure 11-1: Carrier

	ORG4475
A_0	7.8 ± 0.1
B_0	7.8 ± 0.1
K_0	2.3 ± 0.1
F	7.5 ± 0.1
P_1	12.0 ± 0.1
W	16.0 ± 0.3

Table 11-1: Carrier dimensions [mm]

Carrier material: Polystyrene with Carbon (PS+C).

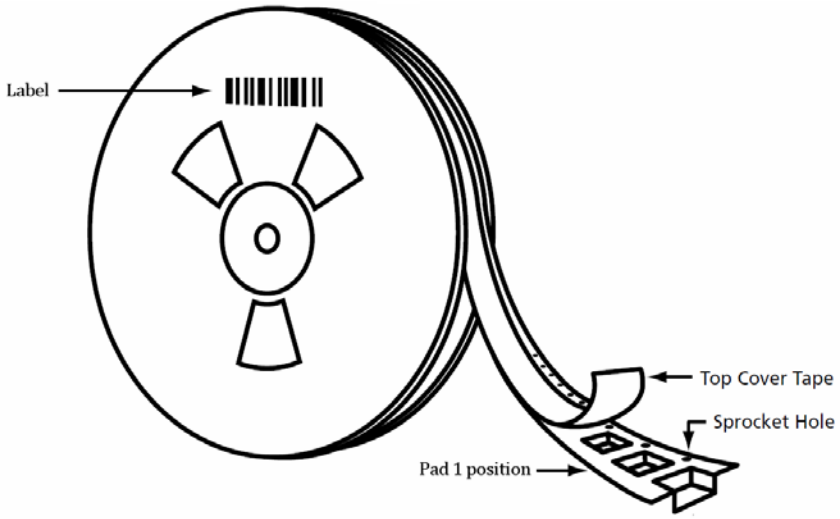

Figure 11-2: Module position

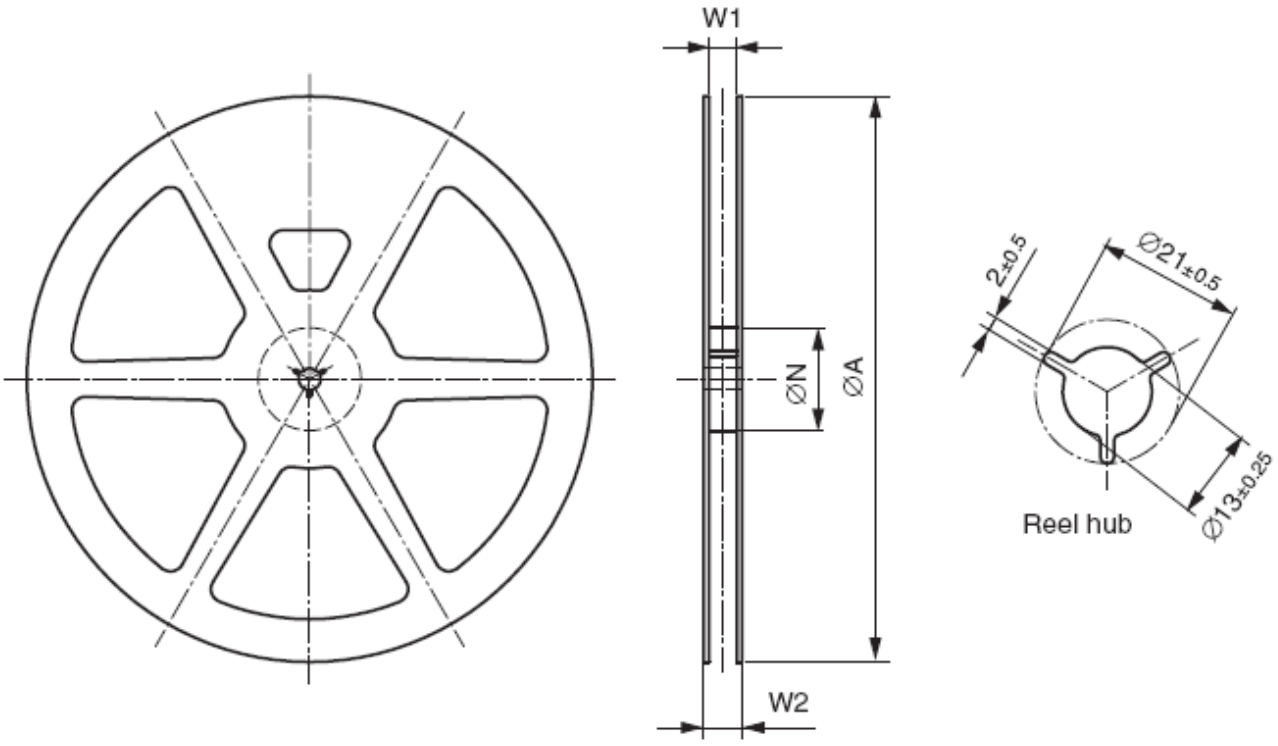

Figure 11-3: Reel

ØA	330 ± 1
ØN	50.0 ± 0.5
W_1	16.5 ± 0.5
W_2	22.0 ± 0.5

Table 11-2: Reel dimensions [mm]

Reel material: Antistatic Plastic.

Units per reel	ORG4475
Standard	500 or 2000

Table 11-3: Reel quantity

11.2 Moisture Sensitivity

The ORG4475 module is Moisture Sensitivity Level (MSL) 3 designated device according to IPC/JEDEC J-STD-033B standard.

Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

11.3 Assembly

The module supports automatic pick-and-place assembly and reflow soldering processes.

Reflow soldering of the module on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

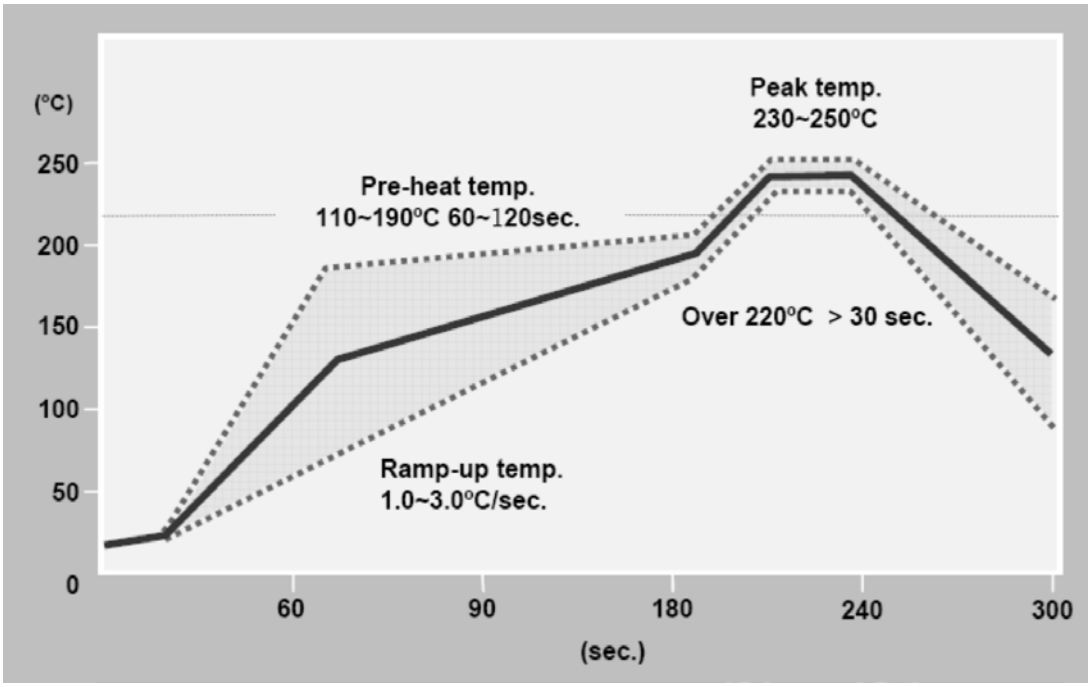

Figure 11-4: Recommended soldering profile

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.

Absolute Maximum reflow temperature is 260°C for 10 sec.

11.4 Rework

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

11.5 ESD Sensitivity

The module is ESD sensitive device and should be handled with care.

11.6 Compliances

The following standards are applied on the production of the ORG4475 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

The modules are manufactured in ISO 9001:2000 accredited facilities.

The modules are manufactured in ISO 14001:2004 accredited facilities.

The modules are designed, manufactured and handled to comply with and according to Pb-Free/RoHS Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

The modules are manufactured in facilities under EU REACH regulation.

The ORG4475 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B
- JAPAN VCCI V-3/2006.04

11.7 Safety Information

Improper handling and use can cause permanent damage to the device.

There is also the possible risk of personal injury from mechanical trauma or shocking hazard.

11.8 Disposal Information

The module and it's integrated products should not be treated as household waste.

For more detailed information about recycling electronic components, please contact your local waste management authority.

12.Mechanical Specifications

- The ORG4475 module has advanced ultra-miniature packaging and a LGA SMD footprint.
- The ORG4475 module size is 5.6mm x 5.6mm.
- The ORG4475 module is Surface Mount Devices (SMD) built on a printed circuit board assembly with a metallic RF enclosure on top of it.
- There are 19 Land Grid Array (LGA) surface mount connection pads with a base metal of copper and an Electroless Nickel / Immersion Gold (ENIG) finish.
- The ORG4475 module supports automated pick and place assembly and reflow soldering processes.

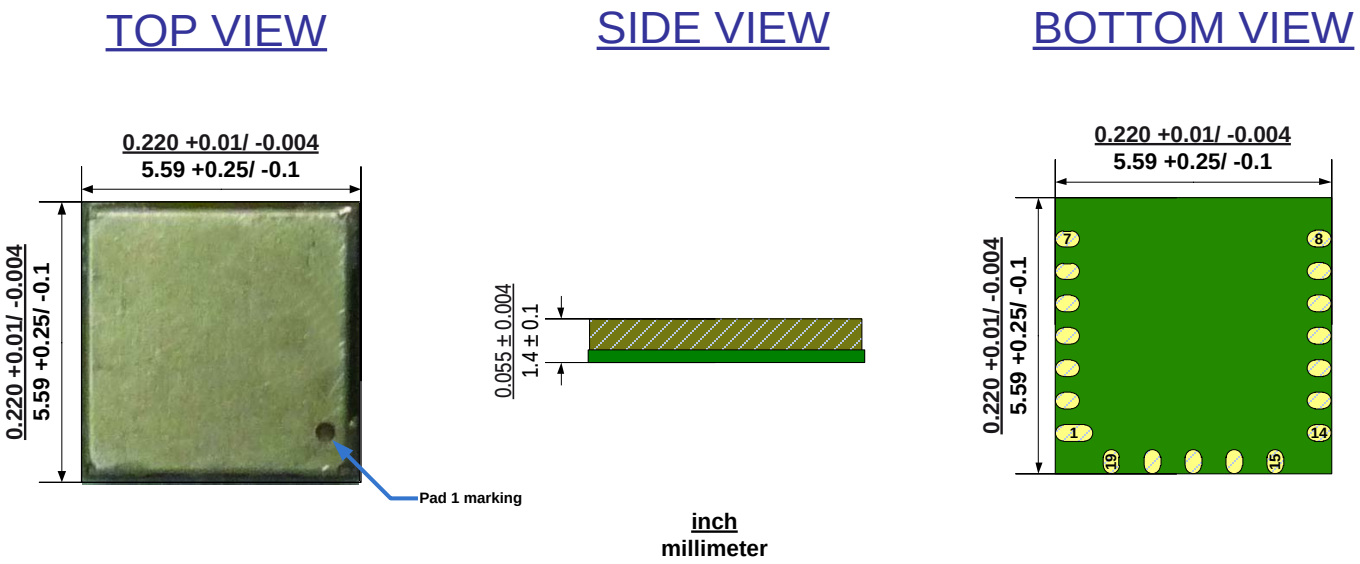

Figure 12-1: ORG4475 mechanical drawing

Dimensions	Length	Width	Height	Weight	
mm	5.59 +0.25/ -0.1	5.59 +0.25/ -0.1	1.4 ± 0.1	gr	0.3
inch	0.220 +0.01/ -0.004	0.220 +0.01/ -0.004	0.055 ± 0.004	oz	0.05

Table 12-1: ORG4475 mechanical information

13.Ordering Information

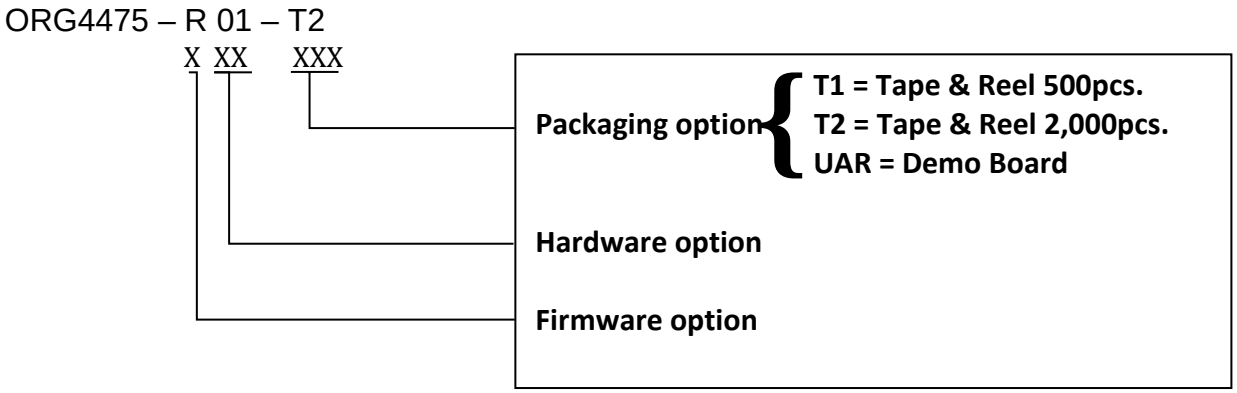

Table 13-1: Ordering options